ANALOG DEVICES

DMT Coprocessor for ADSL Chipset

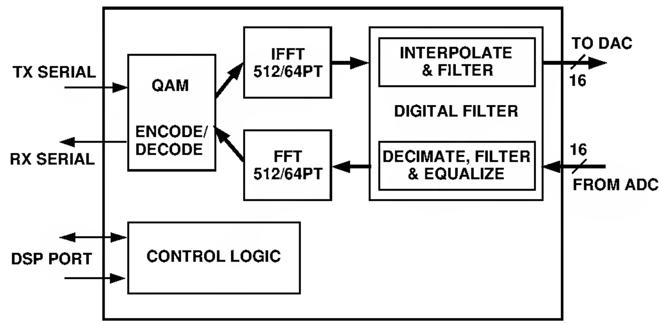
AD6436

FEATURES

Component in Analog Devices DMT ADSL Chipset—AD20msp910
Designed to ANSI/ETSI T1.413 (Cat 1 FDM)
Suitable for CO or Residence (ATU-R and ATU-C)
Performs All DMT Functions and Operations:
- **QAM Encoding and Decoding Operations**
- **Tone Reordering and Scaling**
- **FFT for Receive (512/64 Point at RT/CO)**
- **Inverse FFT on Transmission (512/64 Point)**
- **Frequency and Time Domain Equalization (FDQ and TDQ)**
- **Digital Filters (Interpolation and Decimation)**

128-Lead TQFP
–40°C to +85°C
3.3 V Operation, 600 mW

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD6436 is part of the Analog Devices ADSL chipset, the AD20msp910. It accompanies the AD6435 (Interface and Framer), AD6437 (single-chip analog front end) and ADSP-2183 (control and DSP). Object code is also supplied. Offering a flexible, standard based approach (designed to ANSI T1.413, Category 1 FDM) with low total bill of materials and high performance, the chipset offers a straightforward approach to realizing an ADSL modem.

The AD6436 is a dedicated DMT accelerator, implementing transmit (QAM encode, IFFT, filtering and interpolation filtering) and receive (decimation, filtering and equalization, FFT and QAM decode) operations.

REV. 0

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781/329-4700 World Wide Web Site: http://www.analog.com
Fax: 781/326-8703

AD6436–SPECIFICATIONS

Parameter	Value	Comments
TRANSMIT DAC PORT—DATA WIDTH	16-Bit	
TRANSMIT DAC PORT—RATE CO Mode RT Mode	 17.664 MHz, 8.832 MHz, 4.416 MHz 2.208 MHz, 1.104 MHz, 552 kHz	
RECEIVE ADC PORT—DATA WIDTH	16-Bit	
RECEIVE ADC PORT—RATES	8.832 MHz or 2.208 MHz	At Either CO or RT
DOWNSTREAM FFT/IFFT	512 Points	256 Tones
UPSTREAM FFT/IFFT	64 Points	32 Tones
BITS/CARRIER (MAX)	16	This is more than the fifteen required by ANSI T1.413.
INTERFACE TO AD6435/AD6438	Serial 35.328 MHz	Both Transmit and Receive
POWER SUPPLIES V_{DD} P_{DISS}	 3.3 V ± 10% 600 mW	
TEMPERATURE RANGE	–40°C to +85°C	

Specifications are subject to change without notice.

Timing Specifications

Parameter	Description	Typ	Units
TX Timing			
t_{TX-S}	Setup Time of TX [15:0] from Rising Edge of TX_CLK	12	ns
t_{TX-H}	Hold Time of TX [15:0] from Rising Edge of TX_CLK	12	ns

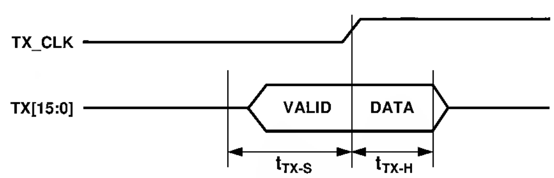


Figure 1. TX Timing

Parameter	Description	Typ	Units
RX Timing			
t_{RX-S}	Setup Time of RX [15:0] from Rising Edge of RX_CLK	5	ns
t_{RX-H}	Hold Time of RX [15:0] from Rising Edge of RX_CLK	0	ns

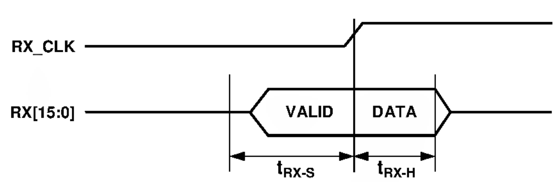


Figure 2. RX Timing

Parameter	Description	Typ	Units
TX Serial I/F Timing			
t_{TFRM-S}	Setup Time of TX_FRM from Falling Edge of TX_RX_SCLK	5	ns
t_{TFRM-H}	Hold Time of TX_FRM from Falling Edge of TX_RX_SCLK	15	ns
$t_{TDREQ-S}$	Setup Time of TX_DREQ from Rising Edge of TX_RX_SCLK	5	ns
$t_{TDREQ-H}$	Hold Time of TX_DREQ from Rising Edge of TX_RX_SCLK	15	ns
t_{TBS-S}	Setup Time of TX_BS from Rising Edge of TX_RX_SCLK	10	ns
t_{TBS-H}	Hold Time of TX_BS from Rising Edge of TX_RX_SCLK	0	ns
t_{TD_S}	Setup Time of TX_SDATA from Rising Edge of TX_RX_SCLK	5	ns
t_{TD_H}	Hold Time of TX_SDATA from Rising Edge of TX_RX_SCLK	0	ns

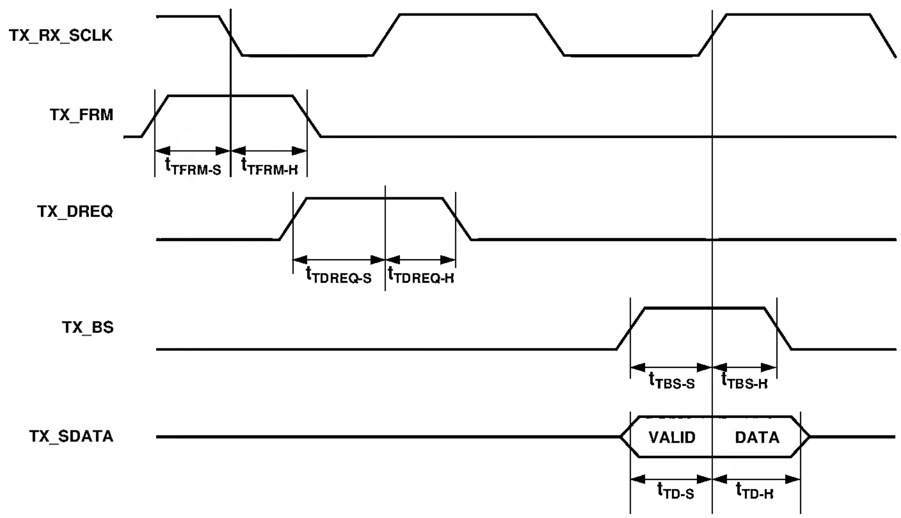


Figure 3. TX Serial I/F Timing

Parameter	Description	Typ	Units
RX Serial I/F Timing			
t_{RFRM-S}	Setup Time of RX_FRM from Falling Edge of TX_RX_SCLK	5	ns
t_{RFRM-H}	Hold Time of RX_FRM from Falling Edge of TX_RX_SCLK	15	ns
$t_{RDREQ-S}$	Setup Time of RX_DREQ from Rising Edge of TX_RX_SCLK	5	ns
$t_{RDREQ-H}$	Hold Time of RX_DREQ from Rising Edge of TX_RX_SCLK	0	ns
t_{RBS-S}	Setup Time of RX_BS from Falling Edge of TX_RX_SCLK	5	ns
t_{RBS-H}	Hold Time of RX_BS from Falling Edge of TX_RX_SCLK	15	ns
t_{RD-S}	Setup Time of RX_SDATA from Falling Edge of TX_RX_SCLK	5	ns
t_{RD-H}	Hold Time of RX_SDATA from Falling Edge of TX_RX_SCLK	15	ns

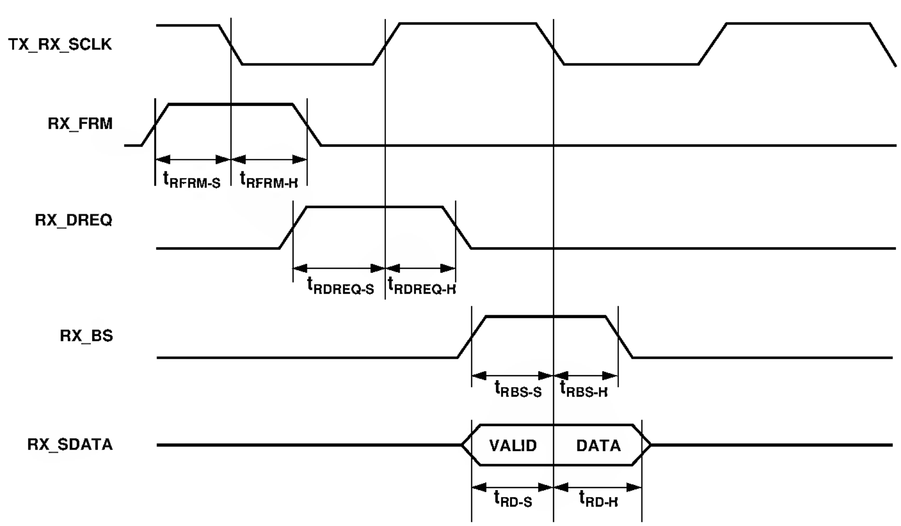


Figure 4. RX Serial I/F Timing

Parameter		Min	Max	Unit
Read Operation				
Timing Requirements:				
t_{RDD}	NRD Low to Data Valid		8	ns
t_{AA}	A0–A13, NCS to Data Valid		14	ns
t_{RDH}	Data Hold from NRD High	0		ns
Switching Characteristics:				
t_{RP}	NRD Pulsewidth	12		ns
t_{CRD}	DSP_CLK High to NRD Low	3	16	ns
t_{ASR}	A0–A13, NCS Setup before NRD Low	2		ns
t_{RDA}	A0–A13, NCS Hold after NRD Deasserted	5		ns
t_{RWR}	NRD High to NRD or NWR Low	12		ns

NOTE:
DSP clock 28 MHz (35.7 ns)

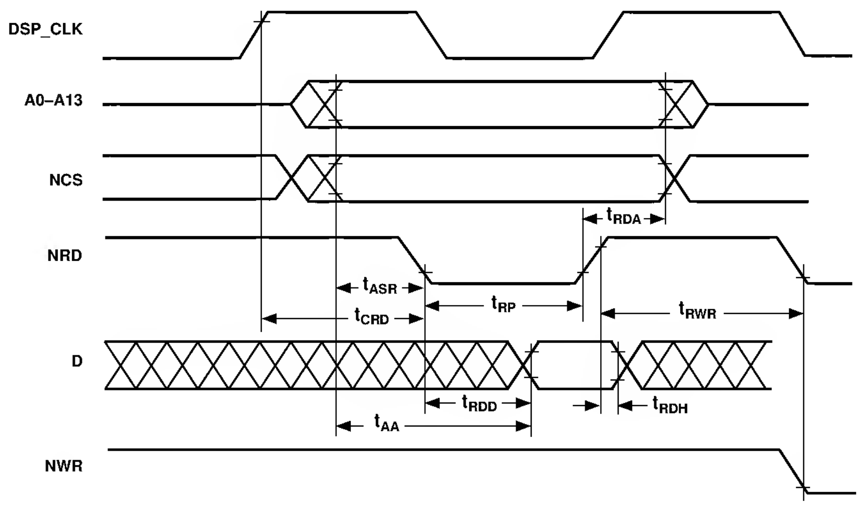


Figure 5. Read Operation

Parameter		Min	Max	Unit
Write Operation				
Switching Characteristics:				
t_{DW}	Data Setup before NWR High	10		ns
t_{DH}	Data Hold after NWR High	6		ns
t_{WP}	NWR Pulsewidth	12		ns
t_{WDE}	NWR Low to Data Enabled	0		ns
t_{ASW}	A0–A13, NCS Setup before NWR Low	2		ns
t_{DDR}	Data Disable before NWR or NRD Low	1		ns
t_{CWR}	DSP_CLK High to NWR Low	3	16	ns
t_{AW}	A0–A13, NCS, Setup before NWR Deasserted	17		ns
t_{WRA}	A0–A13, NCS Hold after NWR Deasserted	5		ns
t_{WWR}	NWR High to NRD or NWR Low	12		ns

NOTE:
DSP clock 28 MHz (35.7 ns)

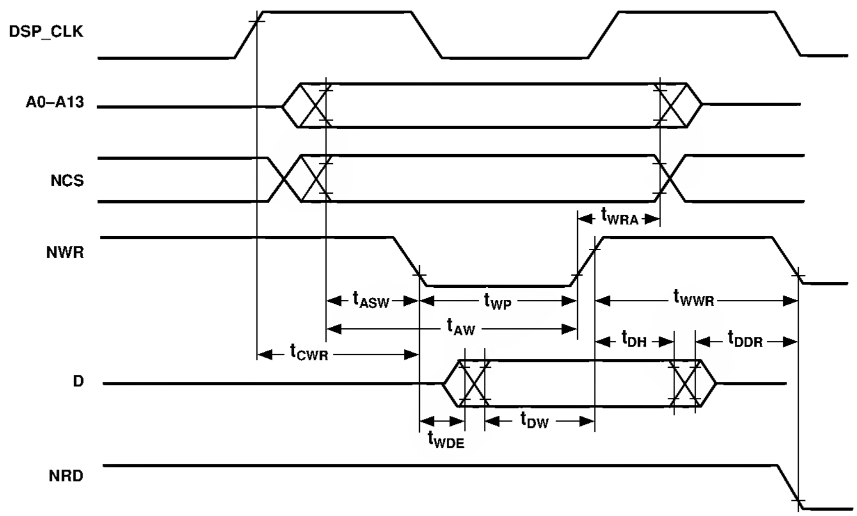


Figure 6. Write Operation

ELECTRICAL SPECIFICATIONS

Parameter	Typ Value	Comments*
V_{OH}	V_{DD}–0.4 V dc	At I_{OH} = –0.5 mA
V_{OL}	0.4 V dc	At I_{OL} = +1.0 mA
V_{IH}	2.0 V dc	
V_{IL}	1.0 V dc	
I_{IH}	±500 nA	V_{IN} = V_{DD} = 3.6 V
I_{IL}	±500 nA	V_{IN} = 0 V, V_{DD} = 3.6 V

*V_{DD} = 3.3 V dc ± 10%.

ABSOLUTE MAXIMUM RATINGS*

Supply Voltage . . . . –0.3 V to +4.6 V
Input Voltage . . . . –0.5 V to V_{DD} + 0.5 V
Output Voltage Swing . . . . –0.5 V to V_{DD} + 0.5 V
Operating Temperature Range (Ambient) . . . . –40°C to +85°C
Storage Temperature Range . . . . –65°C to +150°C
Lead Temperature (5 sec) TQFP . . . . +280°C

*Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD6436	–40°C to +85°C	128-Lead Plastic Thin Quad Flatpack	ST-128

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD6436 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

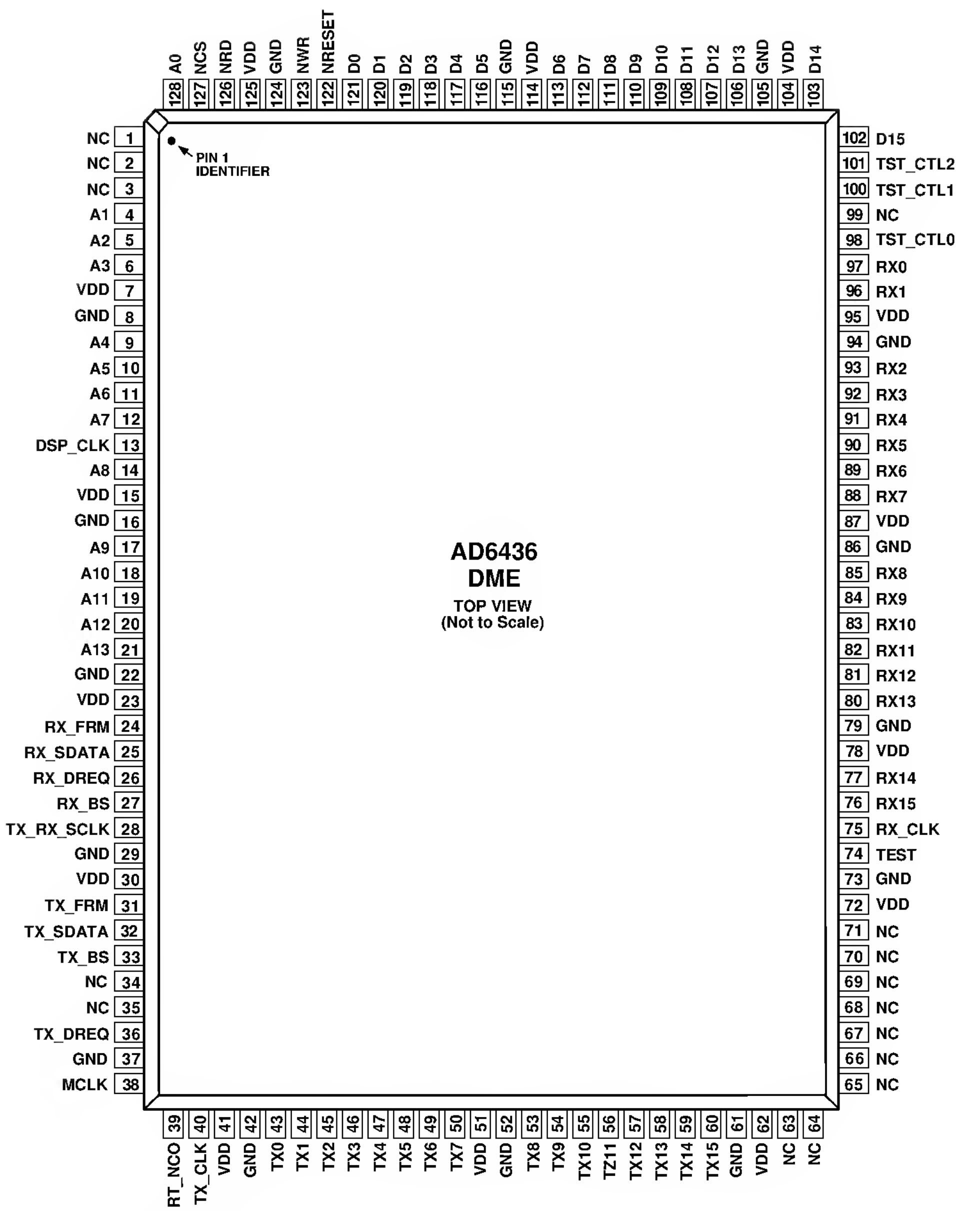
PIN DESCRIPTION

The AD6436 is a 128-lead TQFP. It contains 93 signal pins, 37 output pins, 40 input pins, 16 bidirectional pins and 28 supply pins.

PIN FUNCTION DESCRIPTIONS

Pin No.	Pin Name	Type	Description
1–3, 34, 35, 63–71, 99	NC		Not Connected Pins.
4–6, 9–12, 14, 17–21, 128	A(13:0)	Input	14-Bit Address Bus for DSP Port.
7, 15, 23, 30, 41, 51, 62, 72, 78, 87, 95, 104, 114, 125	VDD	Supply	These pins supply 3.3 V power to the AD6436.
8, 16, 22, 29, 37, 42, 52, 61, 73, 79, 86, 94, 105, 115, 124	GND	Ground	These pins supply ground for the AD6436.
13	DSP_CLK	Input	This comes from the DSP and is used to direct the register ports and for accessing the RAMs.
24	RX_FRM	Output	Frame Pulse for RX Serial Port.
25	RX_SDATA	Output	Serial Data for RX Serial Port.
26	RX_DREQ	Input	Data Request for RX Serial Port.
27	RX_BS	Output	Byte Strobe for RX Serial Port.
28	TX_RX_SCLK	Output	Serial Clock for TX and RX Serial Ports.
31	TX_FRM	Output	Frame Pulse for TX Serial Port.
32	TX_SDATA	Input	Serial Data for TX Serial Port.
33	TX_BS	Input	Byte Strobe for TX Serial Port.
36	TX_DREQ	Output	Data Request for TX Serial Port.
38	MCLK	Input	Master Clock for AD6436 (35.328 MHz).
39	RT_NCO	Input	Mode Pin, 1 = RT Mode; 0 = CO Mode.
40	TX_CLK	Output	Output Clock Used to Qualify Valid Data for DAC.
43–50, 53–60	TX(15:0)	Output	16-Bit Output for Transmit DAC.
74	TEST	Output	Test Pin.
75	RX_CLK	Output	Output Clock Used to Qualify Valid Data for ADC.
76, 77, 80–85, 88–93, 96, 97	RX(15:0)	Input	16-Bit Input from receive ADC.
98, 100, 101	TST_CTL[2:0]	Input	Test Control Pins. These pins are for ADI internal use only. They should be tied low.
102, 103, 106–113, 116–121	D(15:0)	I/O	16-Bit Data Bus from DSP Port.
122	NRESET	Input	Reset Pin, Active Low.
123	NWR	Input	Write Strobe from DSP Port, Active Low.
126	NRD	Input	Read Strobe from DSP Port, Active Low.
127	NCS	Input	Chipset from DSP Port, Active Low.

PIN CONFIGURATION
128-Lead TQFP



NC = NO CONNECT

INTRODUCTION

The AD6436 is one of the ICs that make up the second generation ADSL chipset. The other portions within the AD20msp910 chipset are the AD6435 (which connects to the AD6436, and is responsible for error correction, interleaving and elastic store/framing operations), the AD6437 analog front-end IC, the AD816 driver/receiver and ADSP-2183, which is used as the system control processor. An object code license for all modem software is supplied with the AD20msp910 chipset.

The AD6436 performs the QAM encoding and decoding operations, the frequency domain equalization (FDQ), the FFT and IFFT operations. It also implements a number of digital filter operations including interpolation/decimation and time-domain equalization (TDQ). It is designed to process up to 256 downstream tones (although in a typical system only those numbered 28–255 will be used) and 32 upstream ones (although in a typical implementation only Numbers 8–27 will be used). It is designed to Category 1 of the ANSI/ETSI standard and relies on frequency division multiplexing (FDM) to separate the upstream and downstream signals.

Although the AD6436 is designed as part of the AD20msp910 ADSL chipset, it is suitable for use in other multitone (DMT or OFDM) communication systems.

This data sheet gives a user's description of the AD6436. It describes functionality and interfacing, but does not give any details of the internal structure.

When used as part of the AD20msp910 ADSL chipset, this internal functionality is under the control of the firmware supplied with the ADSP-2183, and the Messaging Protocol (MP) implemented there. This protocol supplies a hardware-neutral method of controlling the operation of the ADSL chipset, which will be compatible between different hardware implementations.

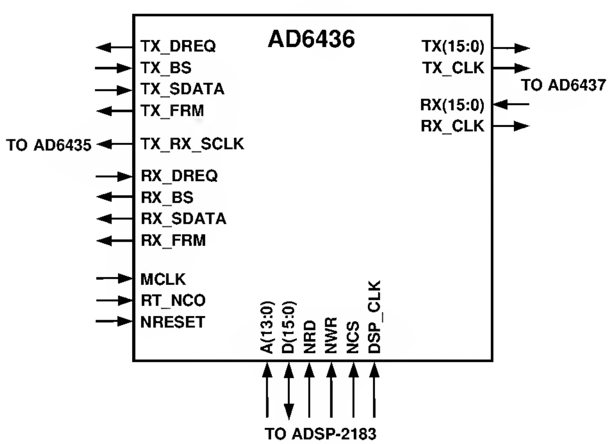


Figure 7. Functional Pin Diagram

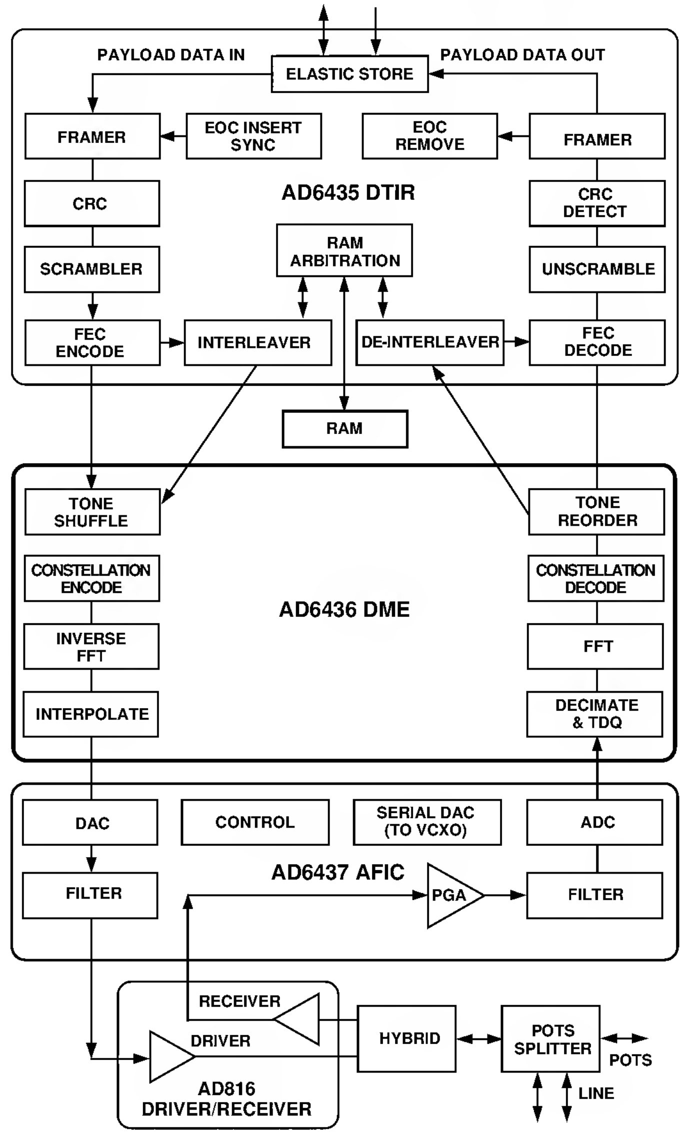


Figure 8. AD20msp910 System Block Diagram

FUNCTIONAL DESCRIPTION

The AD6436 consists of six major blocks: a QAM encoder/decoder block, an FFT block, an IFFT block, a DFIC block, a DSP port control block and a clock control block.

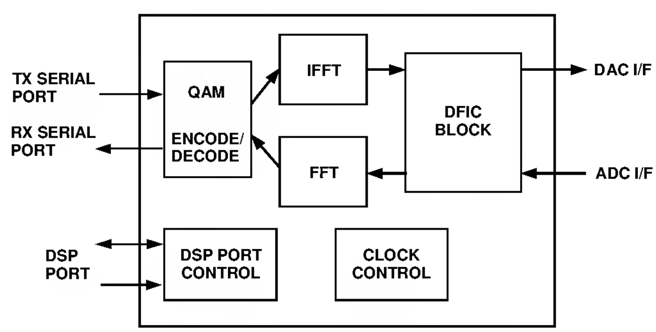


Figure 9. Block Diagram

QAM Encoder/Decoder

The QAM block handles the QAM encoding and decoding of data. It corresponds to the "Tone Ordering" and "Constellation encoder and gain scaling" blocks in the T1.413 reference model.

Data is received from the AD6435/AD6438 at 35.328 MHz as a serial stream, and is fed to the encoder buffer. This block is responsible for the encoding, bin allocation and tone reordering operations. Each subcarrier (from 0 to 255) can handle from 0 to 16 bits, with the density controlled by the bin allocation. This block also handles the pilot tone insertion (Bin 64 in CO mode and Bin 16 in the RT).

The QAM decoder is very similar, recovering the data from the subcarriers and reversing the tone ordering and bit allocation operations. It also operates the same way in CO and RT mode. The receive serial interface between the QAM decoder and the AD6435/AD6438 operates at 35.328 MHz.

IFFT Block

The IFFT block performs a 512-point inverse FFT in CO mode (transmitting the downstream data) and a 64-point inverse FFT in RT mode (transmitting the upstream data). It also implements gain-scaling at this time.

While the data is read out of the IFFT block and into the DFIC, the cyclic prefix is added to the transmit path. The purpose of the cyclic prefix is to make the symbol appear periodic in nature to the receiver. The IFFT produces 512 real data samples in CO mode, to which 32 samples are added, and 64 real data samples in RT mode, to which four are added.

FFT Block

On the receive channel, the FFT block performs a 64-point FFT in CO mode (receiving the upstream duplex data) and a 512-point FFT in RT mode (receiving the downstream simplex data). In addition, carriers can be scaled up to provide full precision for the FDQ and QAM decode operations. After the transform, the FFT performs the FDQ operation in the output buffer. In addition to performing the FFT, this block also strips off the cyclic prefixes and removes the pilot tones from the symbol.

Digital Filter Block

This implements a variety of digital filtering operations, including Time Domain Equalization (TDQ) and the interpolation/decimation tasks that connect the digital devices to the analog stage (AD6437/AD6440).

NB Data Width

The AD6436 uses 16-bit datapaths internally. As such, it may be used with high resolution analog stages with up to 16-bit resolution and take full advantage of them. The AD6437/AD6440—its companion part in the AD20msp910 chipset—is only specified to 12-bit linearity.

INTERFACE TIMING

The AD6436 contains a transmit serial port in which the AD6435/AD6438 transmits a bit stream to the AD6436 and a receive serial port in which AD6435/AD6438 receives a serial bit stream from the AD6436. The AD6436 also interfaces with an ADC and a DAC, and has a DSP host port, which allows a DSP to monitor the AD6436 and control the data through the device.

TX SERIAL PORT

The TX serial interface between the AD6436 and AD6435/AD6438 uses five (5) signals:

TX_RX_SCLK:	Serial clock provided by AD6436.
TX_DREQ:	Data request provided by AD6436.
TX_FRAME:	Frame strobe provided by AD6436.
TX_BS:	Byte strobe provided by AD6435/AD6438.
TX_SDATA:	Serial data provided by AD6435/AD6438.

This is a byte protocol. The AD6436 raises TX_DREQ to request data (ref T0). The AD6435/AD6438 samples the TX_DREQ on its rising clock and when seen, outputs a one clock byte strobe TX_BS (ref T1) and simultaneously places Bit 0 of the byte on the TX_SDATA pin. Then on the next seven rising clocks the AD6435/AD6438 places Bits 1 through 7 on the TX_SDATA pin. On the next rising clock, the TX_DREQ line is again sampled (ref T5), and if high, and another byte is ready to transmit, outputs the byte strobe coincident with the first bit of the next byte, then proceeds to output the reset of the byte in successive clock cycles. If TX_DREQ were low, or another byte was not available yet, the byte strobe would not be output, and TX_DREQ would continue to be sampled on successive rising clock edges while waiting for available data. The AD6435/AD6438 is free to place Bit 0 of a byte on the TX_SDATA pin even if the AD6436 will not be taking it, as long as the byte strobe is not pulsed. Once the byte strobe is pulsed for Bit 0, the TX_DREQ line is ignored until all eight bits are sent.

The AD6436, once TX_DREQ is raised, leaves TX_DREQ high and samples TX_BS on successive rising edges of the clock. Once TX_BS is seen high (ref T2), the AD6436 knows that Bit 0 can be sampled, followed by the remaining seven bits on the next seven rising clocks edges (ref T3). If desired, the TX_DREQ can be dropped at this time. When Bit 6 is being sampled (ref T4), the AD6436 must raise or lower the TX_DREQ line depending on whether it knows it wants another byte immediately following the current byte. This timing is needed to ensure the AD6435/AD6438 will (or will not) see the TX_DREQ signal as it outputs the last bit.

The TX_FRAME signal, which is not shown, is pulsed on the rising edge of the AD6436 clock at the beginning of frame. The AD6435/AD6438 will not respond to the TX_DREQ line before the start of a frame, or after the number of data bytes programmed by the DSP has been transferred within a frame.

RX SERIAL INTERFACE

The RX serial interface between the AD6436 and AD6435/AD6438 uses five (5) signals:

TX_RX_SCLK:	Serial clock provided by AD6436.
RX_FRAME:	Frame strobe provided by AD6436.
RX_BS:	Byte strobe provided by AD6436.
RX_SDATA:	Serial data provided by AD6436.
RX_DREQ:	Data request provided by AD6435/AD6438.

This is a byte protocol. The AD6435/AD6438 raises RX_DREQ to request data (ref T0). The AD6436 samples the RX_DREQ on its rising clock and when seen, outputs a one clock byte strobe RX_BS (ref T1), and at the same time places Bit 0 of the byte on the RX_SDATA pin. Then on the next seven rising clocks the AD6435/AD6438 places Bits 1 through 7 on the RX_SDATA pin. As the last bit is output, the RX_DREQ line is

again sampled (ref T5), and if high, and another byte is ready to transmit, outputs the byte strobe coincident with the first bit of the next byte, then proceeds to output the remainder of the byte in successive clock cycles. If RX_DREQ were low, or another byte not yet available, the byte strobe would not be output, and RX_DREQ would continue to be sampled on successive rising clock edges while waiting for available data. The AD6436 is free to place Bit 0 of the next byte on the pin even if RX_DREQ is low, as long the byte strobe is not pulsed. Once the byte strobe is pulsed for Bit 0, the RX_DREQ line is ignored until all eight bits are sent.

The AD6435/AD6438, once RX_DREQ is raised, leaves RX_DREQ high and samples RX_BS on successive falling edges of the clock. Once RX_BS is seen high (ref T2), the AD6435/AD6438 samples Bit 0 and knows that the data bits can be sampled on the next seven falling clocks edges (ref T3). If desired, the RX_DREQ can be dropped at this time. When Bit 7 is being sampled (ref T4), the AD6435/AD6438 must raise or lower the RX_DREQ line depending on whether it knows it wants another byte immediately following the current byte. This timing is needed to ensure the AD6436 will (or will not) see the RX_DREQ signal on the rising edge after the last bit.

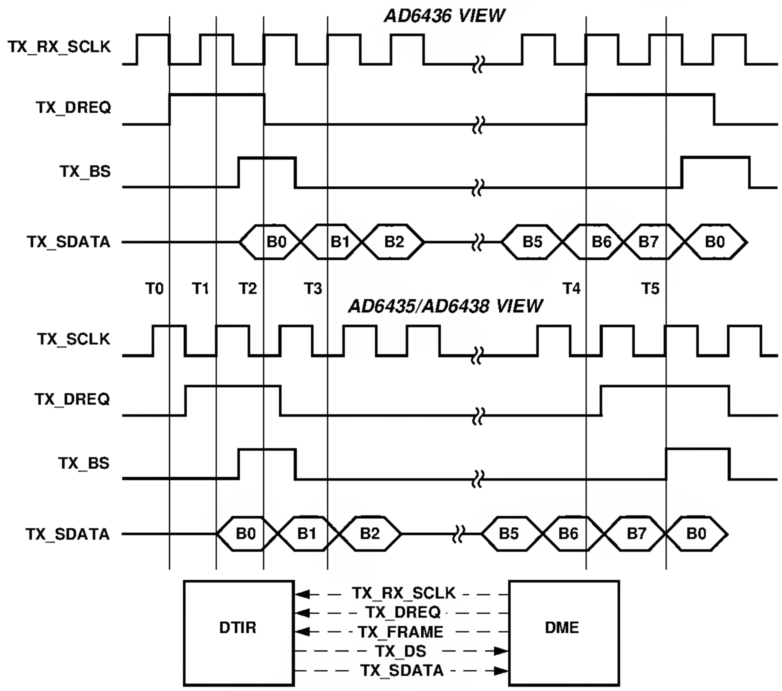


Figure 10. AD6436–AD6435/AD6438 Interface—Transmit

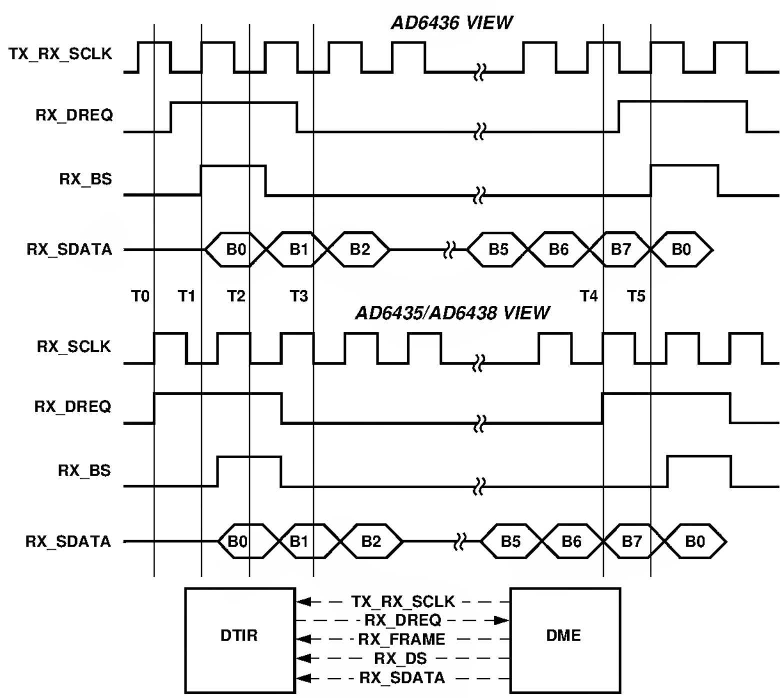


Figure 11. AD6436–AD6435/AD6438 Interface—Receive

The RX_FRAME signal, which is not shown, is pulsed on the rising edge of the AD6436 clock at the beginning of frame. The AD6435/AD6438 will not raise the RX_DREQ line before the start of a frame, or after the number of data bytes programmed by the DSP has been received within a frame.

DAC INTERFACE

The AD6436 provides sixteen bits to an A/D converter. Sample rates of 17.664 MHz, 8.832 MHz and 4.416 MHz can be sent out in CO mode. In RT mode, rates of 2.208 MHz, 1.104 MHz and 552 kHz can be sent out in RT mode. The sample rate is determined by the setting of the programmable down sampler in the DFIC.

Accompanying the 16-bit data is a clock, TX_CLK, to qualify when the data is valid.

All 16 bits are valid, but if the DAC has fewer bits, it is the most significant bits of the word that should be connected to the DAC (i.e., when connecting the AD6436 to the AD6437, Bits D0 and D1 should be left NC). These bits will be used in future, higher precision, analog stages.

ADC INTERFACE

The AD6436 can accept sixteen bits from an A/D converter. The sample rate for both RT and CO mode is 8.832 MHz normally, but can optionally be 2.208 MHz. A signal called RX_CLK is provided to qualify when the A/D converter needs to provide valid data.

All 16 bits are valid, but if the ADC has fewer bits, it is the most significant bits of the word should be connected to the ADC (i.e., when connecting the AD6436 to the AD6437, Bits D0 to D3 should be tied to ground). These bits will be used in future, higher precision, analog stages.

DSP PORT

The DSP port consist of:

A 14-Bit Address Bus, A[13:0]

A 16-Bit Data Bus, D[15:0]

Three Bus Control Pins, NRD, NWR, NCS.

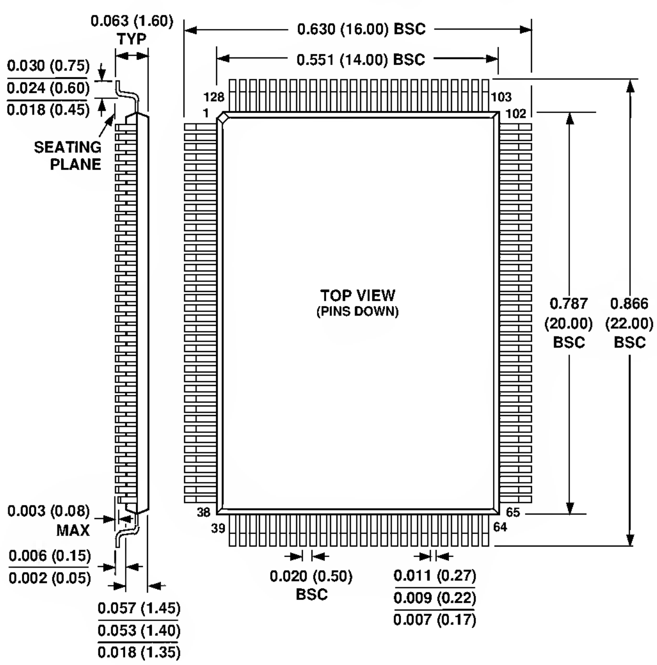
The DSP port allows a 2183 DSP to access the AD6436.

C3229–3–10/97

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

128-Lead Plastic Thin Quad Flatpack (ST-128)



PRINTED IN U.S.A.